WHAT IS CLAIMED IS:

1. A gate driver, comprising:

a gate control signal generator having a first input and configured to output a gate control signal to a power semiconductor switch, the gate control signal generator being provided proximate a high side of the gate driver;

a first sub-circuit having a first signal path and a second signal path that are suitable for transmitting signals, the first and second signal paths coupled to the first input of the gate control signal generator, the second signal path being configured to provide a signal to the first input with a reduced signal delay; and

a comparator configured to receive signals from the high side, the comparator being provided proximate a low side of the gate driver.

2. The gate driver of claim 1, further comprising:

a second sub-circuit coupled to a second input of the gate control signal generator, wherein the first input of the gate control signal generator receives a signal of first voltage from the first sub-circuit and the second input of the gate control signal generator receives a signal of second voltage from the second sub-circuit, wherein the gate control signal generator outputs a gate control signal according to a voltage difference between the signal of first voltage and the signal of second voltage.

3. The gate driver of claim 2, wherein the second sub-circuit includes a third signal path and a fourth signal path that are suitable for transmitting signals, the third and fourth signal paths coupled to the second input of the gate control signal generator.

4. The gate driver of claim 3, wherein the second signal path and fourth signal path are feed forward connections.

5. The gate driver of claim 1, wherein the first signal path of the first sub-circuit includes a first resistor with a first end configured to receive an input signal and a second end configured to output a signal of first voltage to the first input of the signal generator, and the second signal path including a first capacitor having a first end and a second end, the first end of the first capacitor being electrically coupled to the first end of the first resistor and the second end of the first capacitor being electrically coupled to the second end of the first resistor.

6. The gate driver of claim 5, further comprising:

a second sub-circuit including a third signal path and a fourth signal path that are suitable for transmitting signals, the third and fourth signal paths coupled to a second input of the gate control signal generator.

7. The gate driver of claim 6, wherein the third signal path of the second sub-circuit includes a second resistor with a first end configured to receive an input signal and a second end configured to output a signal of second voltage to the second input of the signal generator, and the fourth signal path including a second capacitor having a first end and a second end, the first end of the second capacitor being electrically coupled to the first end of the second resistor and the second end of the second capacitor being electrically coupled to the second end of the second resistor.

8. The gate driver of claim 1, further comprising:

a second sub-circuit having a third signal path and a fourth signal path that are suitable for transmitting signals, the third and fourth signal paths coupled to the second input of the gate control signal generator, the fourth signal path being configured to provide a signal to the second input with a reduced signal delay;

a third sub-circuit provided in series between the first sub-circuit and the first input of the gate control signal generator, the third sub-circuit including a fifth signal path and a sixth signal path coupled to the first input of the gate control signal generator; and

a fourth sub-circuit provided in series between the second sub-circuit and the second input of the gate control signal generator, the fourth sub-circuit including a seventh signal path and a eighth signal path coupled to the second input of the gate control signal generator.

9. The gate driver of claim 8, wherein the third and fourth sub-circuits provide the gate driver with an increased breakdown voltage.

10. A power module having a high side device and a low side device, comprising:

a gate control signal generator having a first input and configured to output a gate control signal to a power semiconductor switch, the gate control signal generator being provided within the high side device;

a first sub-circuit having a first signal path and a second signal path that are suitable for transmitting signals, the first and second signal paths coupled to the first input of the gate control signal generator, the second signal path being configured to provide a signal to the first input with a reduced signal delay;

a second sub-circuit includes a third signal path and a fourth signal path that are suitable for transmitting signals, the third and fourth signal paths coupled to the second input of the gate control signal generator;

a comparator configured to receive signals from the high side device, the comparator provided at the low side device,

wherein the first input of the gate control signal generator receives a signal of first voltage from the first sub-circuit and the second input of the gate control signal generator receives a signal of second voltage from the second sub-circuit,

wherein the gate control signal generator outputs a gate control signal according to a voltage difference between the signal of first voltage and the signal of second voltage,

wherein the second signal path and fourth signal path are feed forward connections.

11. The module of claim 10, wherein the first signal path of the first sub-circuit includes a first resistor with a first end configured to receive an input signal and a second end configured to output a signal of first voltage to the first input of the signal generator, and the second signal path including a first capacitor having a first end and a second end, the first end of the first capacitor being electrically coupled to the first end of the first resistor and the second end of the first capacitor being electrically coupled to the second end of the first resistor.

12. The module of claim 10, wherein the third signal path of the second sub-circuit includes a second resistor with a first end configured to receive an input signal and a second end configured to output a signal of second voltage to the second input of the signal generator, and the fourth signal path including a second capacitor having a first end and a second end, the first end of the second capacitor being electrically coupled to the first end of the second resistor and the second end of the second capacitor being electrically coupled to the second end of the second resistor.

13. The module of claim 10, further comprising:

a third sub-circuit provided in series between the first sub-circuit and the first input of the gate control signal generator, the third sub-circuit including a fifth signal path and a sixth signal path coupled to the first input of the gate control signal generator; and

a fourth sub-circuit provided in series between the second sub-circuit and the second input of the gate control signal generator, the fourth sub-circuit including a seventh signal path and a eighth signal path coupled to the second input of the gate control signal generator,

wherein the third and fourth sub-circuits provide the gate driver with an increased breakdown voltage.

14. The module of claim 10, further comprising:

a first communication circuit configured to receive a first communication signal;

a second communication circuit configured to receive a second communication signal;

a third communication circuit configured to receive the first communication signal; and

a fourth communication circuit configured to receive the second communication signal,

wherein the first and second communication signals are received at the first input node of the signal control generator to cancel each other, the first and second communication signals are received at the second input node of the signal control generator to cancel each other, and

wherein the first and second communication signals are configured to be input to first and second input of the comparator provided at the low side device, respectively.